REMARKS

Claims 3, 4, 6, 10-11, 15, and 21-22 are amended, no claims are canceled, and claims 27-29 are added; as a result, claims 1-29 are now pending in this application.

§*102 Rejection of the Claims*

Claims 1-2, 8-9, 13-14, 18, and 20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wyland *et al.* (U.S. 6,205,462). Applicant does not admit that Wyland *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. § 1.131, to antedate Wyland *et al.* However, Applicant also urges that the claims distinguish the reference, and therefore respectfully traverses the rejections of claims 1-2, 8-9, 13-14, 18, and 20.

Independent claim 1

Claim 1 recites, "a floating point conversion unit to convert the product from the first exponent weight to a converted product with a second exponent weight." (emphasis added) The specification of the present application on page 7, lines 2-15 states:

> The exponent of the product, E_p, is an eight bit number with a least significant bit weight equal to one. For example, an E_p field of 00000011 has a value of three, because the least significant bit has a weight of one, and the next more significant bit has a weight of two. For the purposes of this description, this exponent format is termed "base 2," and the product is said to be in base 2. Floating point conversion unit 220 converts the product from base 2 to a different base. For example, exponent path 312 is an exponent conversion unit that sets the least significant five bits of the exponent field to zero, and truncates the exponent field to three bits, leaving the least significant bit of the exponent of the converted product, E_{cp}, with a weight of 32. For example, an E_{cp} field of 011 has a value of 96, because the least significant bit has a weight of 32, and the next more significant bit has a weight of 64. For the purposes of this description, this exponent format is termed "base 32," and the converted product is said to be in base 32. (emphasis added)

Therefore, the floating point conversion unit converts the product from a product having an exponent with a first exponent weight to a product with a second exponent weight. In contrast, Wyland *et al.* at column 4, lines 20-27, states, "Exponent sum 141 generated by adder 140 is the sum of two exponents E1 and E2 and hence represents the exponent of mantissa product 143.

With the sum of exponents and final fixed point data format known, the necessary number of shifting places for the product of mantissas can be calculated and, therefore, shifter 144 can be designed accordingly to implement this shifting." Hence, Wyland *et al.* teaches an "exponent sum generated by adder 140," but fails to teach "a second exponent weight" for the exponent, and therefore fails to teach each of the elements of claim 1. In response to this argument, the Office Action on page 7 states,

> The examiner respectfully submits that the case for converting the product from the first exponent weight to a converted product with a second exponent weight is seen whenever the input operands are integers. The output of exponent product of integers have to convert to a special floating-point exponent format as seen in Figure 1E. Thus, it is clearly seen that there is a converson unit to convert the product from the first exponent weight (e.g. Figure 1B) to a converted product with a second exponent weight (e.g. Figure 1E).

Applicant respectfully disagrees for several reasons. First, Wyland *et al.* at column 2, lines 52-56 recites, "In the present invention, integers and floating point numbers are represented in a special combined data format. With reference to FIG. 1A, each number in the special combined data format, for illustrative purpose, has an 8-bit exponent (bits 23 to 30) and a 24-bit mantissa (bits 0 to 22 and bit 31)." Therefore, Wyland *et al.* teaches that both integers and floating point number have the same format, including an 8-bit exponent. Wyland *et al.* describes FIG 1 B at column 2, lines 57-64 which recites,

> With reference to FIG. 1B, the number is an integer. Its 24-bit "mantissa" (bits 0 to 22 and bit 31) is in 2-complement format. Its 8-bit "exponent" (bits 23 to 30) is filled with the value of bit 31, i.e. all zeros if the integer is positive and all ones if negative. So, this 32-bit special format can represent integers in a range from -2^{23} to 2^{23} -1. This range corresponds to 2^{24} different integer representations.

Thus, FIG 1B is merely a description of how an integer is represented in the special format used by Wyland *et al.* Wyland *et al.* describes FIG 1E at column 3, lines 17-20 wherein, "With reference to FIG. 1E, the number is a floating point number; its 24-bit 'mantissa' (bits 0 to 22 and bit 31) in the special combined data format contains its 23-bit actual mantissa (bits 0 to 22) and its sign (bit 31)," and further, at column 3, lines 25-26, "The floating point number's 8-bit 'exponent' (bits 23 to 30) is in offset format." (emphasis added)

Therefore, in Wyland *et al.* FIG. 1B represents a integer in special format, including an 8 bit exponent, and FIG 1E represents a floating point number in special format, including an 8 bit exponent. Thus, FIG. 1E is not a "converted product with a second weight" of FIG 1B, as suggested in the Office Action, but both figures represent two types of numbers represented in the same special format, the special format including the representation with regards to the exponent's format.

Second, any conversion disclosed in Wyland *et al.* occurs before a product is generated, and thus can not teach a floating point conversion unit "to convert the product" from the first exponent weight to a "converted product" with a second exponent weight, as recited in claim 1 of the present application. Wyland *et al.* at column 3, lines 46-52 recites,

> Multiply-Accumulate circuit 100 includes four input registers 102, 104, 106, and 108 for receiving as input two operands in the special combined data format. Eight-bit exponents E1 and E2 of the first and second operands are loaded into input registers 102 and 104, respectively. Mantissas M1 and M2 of the first and second operands are loaded into input registers 106 and 108, respectively. (emphasis added)

Thus, Wyland *et al.* discloses that all operands input into the Multiply-Accumulate circuit 100 must be in special combined data format, and so any integer operands must already be converted into the special combined data format *before* any output, such as a product of the operands, is generated. Thus, Wyland *et al.* fails to teach "The output of exponent product of integers have to convert to a special floating-point exponent format as seen in Figure 1E" as suggested on page 7 of the Office Action, because Wyland *et al.* does not generate any output of exponent product integers, and only discloses generating outputs based on the input of operands in the special combined data format.

Third, Wyland *et al.* at column 4, lines 20-27 states, "Exponent sum 141 generated by adder 140 is the sum of two exponents E1 and E2 and hence represents the exponent of mantissa product 143. With the sum of exponents and final fixed point data format known, the necessary number of shifting places for the product of mantissas can be calculated and, therefore, shifter 144 can be designed accordingly to implement this shifting." However, there is no teaching in Wyland *et al.* that the exponent sum generated by adder 140 has a different exponent weight than either of the two exponents E1 or E2. Further, there is no teaching in Wyland *et al.* that the *product* of shifter 144 will have an exponent weight that is different from the exponent sum

generated by adder 140. Hence, Wyland *et al.* discloses an "exponent sum generated by adder 140," but fails to teach to convert the product from the first exponent weight to a converted product with a second exponent weight as recited in claim 1 of the present application.

Thus, Wyland *et al.* fails to teach each of the elements of claim 1, and so the Office Action fails to state a *prima facie* case of anticipation with respect to claim 1. For the above and other reasons, Applicant urges that claim 1 meets all the statutory requirements, and ought to be allowed. Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claim 1.

Dependent claims 2 and 8

Claims 2 and 8 depend from claim 1, and so include all of the elements recited in claim 1. A stated in connection with claim 1, Wyland *et al.* fails to teach each of the elements of claims 2 and 8. Thus, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 2 and 8. For the above and other reasons, Applicant urges that claims 2 and 8 meet all the statutory requirements, and ought to be allowed. Therefore, Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of claims 2 and 8.

Independent claims 9 and 18; Dependent claims 13 and 20

Independent claim 9 recites, "an exponent conversion unit coupled to the output of the exponent summer, to convert the product exponent to a second weight." Further, independent claim 18 recites, "converting the product to have a different least significant bit weight exponent field." As stated in connection with claim 1, Applicant submits that Wyland *et al.* fails to teach an exponent conversion unit coupled to the output of the exponent summer, to convert the product exponent to a second weight, and fails to teach converting the product to have a different least significant bit weight exponent field, as recited in claims 9 and 18 respectively, and so fails to teach each of the elements of claims 9 and 18. Thus, the Office Action fails to state a *prima facie* case of anticipation with respect to claims 9 and 18.

Claims 13 and 14 depend from claim 9, and claim 20 depends from claim 18. As stated above with regards to claims 1, 9, and 18 and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of anticipation with respect to

claims 13-14 and 20. For the above and other reasons, Applicant urges that claims 9, 13-14, 18, and 20 meet all the statutory requirements, and ought to be allowed. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 9, 13-14, 18, and 20.

§103 Rejection of the Claims

Claims 12, 16-17, and 19 were rejected under 35 U.S.C. § 103(a) as being obvious over Wyland *et al.* (U.S. 6,205,462) in view of Dibrino *et al.* (U.S. 6,542,915). Applicant does not admit that either Wyland *et al.* or Dibrino *et al.* is prior art and reserves the right to antedate Wyland *et al.* and Dibrino *et al.* as provided for under 37 C.F.R. § 1.131. However, Applicant also asserts that the rejected claims distinguish any combination of the references that might be proper under 35 U.S.C. § 103, and so respectfully traverses the rejections of claims 12, 16-17, and 19.

Claims 12 and 16-17 depend from claim 9, and therefore include all the elements of claim 9. Claim 19 depends from claim 18, and therefore includes all the elements of claim 18. As noted above, claim 9 recites, "an exponent conversion unit coupled to the output of the exponent summer, to convert the product exponent to a second weight," and claim 18 recites, "converting the product to have a different least significant bit weight exponent field."

As stated in connection with claims 1, 9, and 18 above, Wyland *et al.* fails to teach or suggest these elements. Further, Applicant does not find in Dibrino *et al.* these elements missing from Wyland *et al.* Instead, Dibrino *et al.* at column 2, lines 62-64, states, "FIG. 1 illustrates a typical floating-point pipeline. This diagram shows the 'Mantissa' dataflow only (the exponent dataflow logic is not shown)," and at column 6, lines 63-66, " FIG. 8 represents pipeline stage 2 of the floating-point pipeline of FIG. 1 with the prior art two-input LZA block 101 replaced by the new 'high-order' LZA 801, with N=5 (A five-input LZA)," and at column 7, lines 4-5, "Elements 804,807, 808, 809, 810 operate similarly to blocks 104, 107, 108, 109, 110." Hence, Dibrino *et al.* also fails to teach or suggest each of the elements as recited in claims 9 and 18.

Thus, neither Wyland *et al.* nor Dibrino *et al.*, either alone or in combination, teach or suggest each of the elements of claims 9 and 18, so the Office Action fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19.

Further, the cited documents themselves teach away from making the combination of Wyland *et al.* and Dibrino *et al*, as suggested by the Office Action. Wyland *et al.* at column 4, lines 35-51 discloses that the shifter produces a final 48.32 fixed point data format, so that shifter 144 can be pipelined, and further, that the operational product generated by the shifter is led to full adder 148. In contrast, Dibrino *et al.* at column 3, lines 28-35 recites,

> It is important to note that the A*C product is 48 bits wide with at most two bits to the left of the implied decimal point. Any bits of the shifted B-operand that are to the left of these two bits do not require a full adder. Instead, these bits to the left of A*C require only to be incremented if the carry-out of the adder is a "1". This is the reason for the incrementer 107 and the mux 108.

Thus, Dibrino *et al.* discloses a 48 bit wide product, with at most two bits to the left of the implied decimal point, wherein Wyland *et al.* requires a 48.32 fixed point format. Therefore, there is no indication that the disclosure in FIG 1B of Dibrino *et al.* is even compatible with the fixed point data format of Wyland *et al.* In addition, Dibrino *et al.* teaches away from the use of the full adder as disclosed in Wyland *et al.*, because Dibrino *et al.* discloses using the different format from Wyland *et al.* Further, Dibrino *et al.* discloses additional circuitry in incrementer 107 and mux 108, which contradicts that statement in the Office Action on pages 4-5 that suggests that the combination Dibrino *et al.* and Wyland *et al.* would "reduce the circuitry."

Therefore, the Office Action fails to provide a proper basis for making the combination of Wyland *et al.* with Dibrino *et al.* and so fails to state a *prima facie* case of obviousness with respect to claims 12, 16-17, and 19. For the above and other reasons, Applicant urges that claims 12, 16-17, and 19 meet all the statutory requirements, and ought to be allowed. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 12, 16-17, and 19.

Double Patenting Rejection

Claims 9-14, 16, and 18-26 were rejected under the judicially created doctrine of double patenting over claims 1, 3-6, 9, and 11-18 respectively of U.S. Patent No. 6,779,013. The Terminal Disclaimer submitted herewith cures this rejection, thus rendering claims 9-14, 16, and 18-26 allowable.

In addition, claims 10, 21, and 22 have been rewritten in independent form. Claim 11 has been rewritten to depend from rewritten claim 10. New claim 29 depends from rewritten claim 21.

Allowable Subject Matter

Claims 3-7 and 15 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3, 4, 6, and 15 have been rewritten in independent form. Claim 5 has not been rewritten in independent form, but depends from rewritten claim 4. Claim 7 has not been rewritten in independent form, but depends from rewritten claim 6. In addition, new claim 27 depends from rewritten claim 3, and new claim 28 depends from rewritten claim 15.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, J. Michael Anglin at (612) 373-6971 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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